

Revision

6

# D F M

Design For Manufacturability

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*Introduction*

This document can be used as a tool to aid in bare printed circuit board design and layout. Incorporating DFM into PCB design and layout, offers many benefits, as listed below (but not limited too):

- Better yields
- Lower costs
- Improved lead times
- Optimal quality

We can achieve the above benefits when the circuit board design incorporates and/or keeps within the tolerances and limitations of the fabricators processes. The key area's of concern include:

- Gerber files
- Fabrication Drawing
- Material (and utilization)
- Line widths and spacing
- Drill
- Multilayers
- Screening (soldermask & nomenclature)
- Metalization / Surface Finishes

The next few pages will address these concerns.

## **GERBER FILES**

In order to manufacture PCBs, it is necessary to have a means of tooling. Most PCB manufacturer's prefer Gerber files. The data contained within the Gerber set should include:

- A. Each individual Copper layer.
- B. Soldermask file for top and bottom layer (if S/M is required)
- C. Silk-screen file for top and bottom layer (if silk-screen is to be used).
- D. Solder paste file for top and bottom layer (if the PCB fabricator is to panelize, the step and repeat paste files can be sent back for stencil fabrication – solder paste files only apply to those designs which incorporate SMT or BGA features).
- E. Fabrication drawing (see following section) or readme file (text document) which will specify parameters for fabrication.
- F. NC drill data (prefer ASCII format).
- G. Aperture list. (Should include decode, size and shape).
- H. IPC-356D for net list test.

*Autocad data is acceptable if Gerber files can not be provided. Our preference is .dxf, .dwg and .hpg, respectively. Apertures are not used in Autocad, however NC drill data and fabrication drawing or readme file should be included.*

To help expedite the accuracy and efficiency of tooling, we encourage the designer to output the Gerber file in a RS-274X output. This will eliminate the need for the PCB manufacturer to load apertures during the tooling process. When sending Gerber files, especially as email attachments, it is strongly recommended that all files are zipped together. One additional note; name the zip file as your bare PCB part number and the revision level. For instance, if your P/N is XXXXX and is at revision 0, then naming your zip file XXXXXRev0.zip or XXXXX0.zip will aid in correct archiving of your P/N's and revisions.

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## **FABRICATION DRAWING**

When data is received, it is important that the manufacturer understand the parameters of the design. These parameters can also be simply stated in a text file, usually named “readme.txt”. The list below will give the essentials for proper fabrication, but as designs can be unique, additional parameters may be necessary that are not discussed below (see attachment A for a sample PCB fab drawing).

- 1) Part Number – it is recommended that the P/N be put on the fabrication drawing or in the readme file. Also, the same P/N should be added to the solder side Copper etch, which will help identify the PCB.
- 2) Revision – as with the P/N, revision should be added to the drawing and often times should be added to the PCB Copper etch, usually placed next to the bare PCB P/N.
- 3) Thickness – the industry standard is to measure thickness “metal to metal”. Most PCBs range from 0.031” to 0.125”. The standard sizes between include 0.047”, 0.062” and 0.093”, however when designing multilayer PCBs thickness can vary depending on impedance requirements, which therefore dictate the dielectric thickness’s selected (see material and utilization for additional information). Cost usually increases as the thickness increases. The most commonly used thickness is 0.062”, which makes it cost effective, yet rigid enough for most applications. PCB thickness tolerance is usually +/- 10% unless otherwise specified.
- 4) Material – since material selection is a significant cost driver, there is much to consider. Most applications require FR4 with a Tg140 rating. The typical dk is 4.2~4.5. This can be specified as “FR4 Tg140” on the fabrication drawing or readme file. For more detailed information on material, see material and utilization section.
- 5) Mechanical – if a PCB does not have a mechanical drawing, then we usually will route or cut out the PCB according to the shear line in the Gerber files. It is recommended that a mechanical drawing also be included (if only a readme file is provided, then the overall dimensions can be specified). The mechanical drawing should not only specify length, width and dimensions of critical features, but it should also reference a feature within the shear line in relation to the overall dimensions (i.e. reference a drilled hole location in relation to the PCB edge). If the PCBs are to be delivered as an array for assembly, then the

mechanical drawing for the array should be included as well. The overall tolerance for mechanical dimensions are +/- 0.005”.

- 6) Drill Chart – most drill charts or drill maps include:
- Drill size
  - Drill quantity
  - Drill symbol
  - Identification as PTH (plated through hole) or NPTH (non-plated through hole).

SIZE	QTY	SYM	PTH
0.012	1296	+	Yes
0.032	346	x	Yes
0.125	4	z	No

Standard tolerance on PTH is +/- 0.003” and for NPTH is +/- 0.002”, which is understood, unless otherwise noted. It is important to note that hole sizes should be specified as finished hole sizes.

- 7) Copper – standard Copper weight for outer layers is 0.5oz and for internal layers is 1oz. Since internal layers do not get plated with additional metal, they remain at 1oz. However, external layers should get plated with a minimum of 1 mil of Copper, thereby making the finished Copper 1 ½ oz. When specifying Copper weight on the base laminate material, it is understood that this is prior to plating. Additional plating should be specified as 1 mil.
- 8) Surface finish – this is the desired finish which is put over the Copper pads. There are many surface finishes available. When choosing a surface finish it is important to understand the assembly process’s and cost considerations for each. The below table is in order from most competitive to less competitive surface finishes:

Finish	Thickness	Positive	Negative
HASL*	50~500u''	Very cost effective, excellent solderability, excellent shelf life	Not as good for 25 mil pitch or less due to thickness variance
Imm. Silver**	10~25u''	Cost effective, good solderability, excellent planor pads	Handle and package carefully
White Tin	10~25u''	Cost effective, excellent planor pads	Handle and package carefully, occasional solderability issues
ENIG***	3~8u'' Au / 150u'' Ni	Excellent solderability, excellent planor pads	Not very cost effective
OSP****	Less than 20u''	Excellent planor pads and good solderability, environmentally friendly	Must process and handle carefully

\* Hot Air Solder Level (Tin/Lead)

\*\* Immersion Silver

\*\*\* Electroless Nickel / Immersion Gold

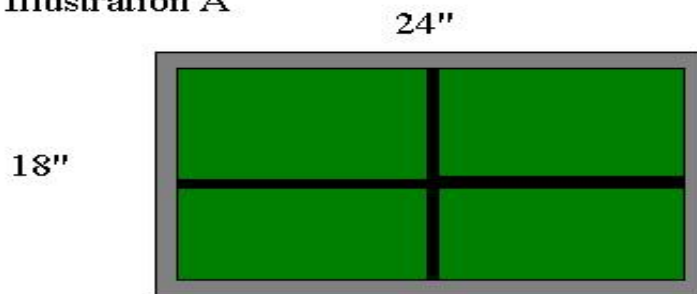
\*\*\*\* Organic Surface Protectant

- 9) Soldermask – the drawing should specify LPI mask (liquid photoimageable) and the color, if it is used. Green is the most commonly used, however blue, red, black and yellow are also available.
- 10) Silk-screen – the drawing should specify if silk-screen is used on one or two sides and the color for the silk-screen. White is the most commonly used.
- 11) Special features (TDR, BBV, BC, etc...) – if the design requires controlled impedance, blind and/or buried via's, buried capacitance, etc...then it should be noted on the fabrication drawing or included in the readme.txt file.

**MATERIAL (AND UTILIZATION)**

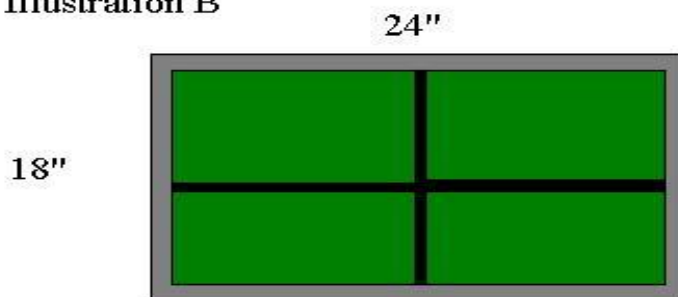
Material and material utilization are two of the biggest cost drivers for printed circuit boards. First we will explore material. The best value material used for IPC classes II and III applications would be FR4 Tg140. For better Z-axis stability FR4 Tg170 may be specified, but it does go up approximately twenty percent in cost. Other materials include Polyimide, Teflon, Duriod and Getek. Since FR4 is limited in its maximum operating temperature, dk (dielectric constant), high moisture and loss, the other materials may be better suited for specific applications, although the cost is typically fifty to three hundred percent greater. As there are many parameters in selecting the right material for specific applications, it is best to contact the manufacturer to discuss the most cost effective solution if the typical FR4 will not meet the application. Regardless of material selection, the material utilization has a direct relationship to the cost of the individual PCB. In other words, the more PCB's that fit efficiently on the panel, the better the cost efficiency will become. Most manufacturer's buy their material in sheet sizes of 36" x 48" or 42" x 48" and then shear the material into a workable size, which is called a panel. Obviously, those panel sizes that can derive evenly into the sheet size produce the most cost effective PCBs. For Q-Fab, we purchase 36" x 48" sheet sizes and therefore dimensions of 12", 16", 18" and 24" are efficient. However, since we require tooling and plating area's on the panel, the engineer must design the PCBs to fit within the workable area of the panel. For single and double sided PCBs we require a 1" border (see illustration A) and for multilayer PCBs we require a 2" border (see illustration B). Please keep in mind that if the PCBs are to be delivered as an array, for assembly purposes, that the array needs to fit within the workable area. Spacing between individual PCB's or arrays on the panel should be a minimum of 0.093" and is typically 0.100" to allow for the router to cut out the individual PCBs or arrays. Our best panel size is achieved with as an 18" x 24".

Illustration A



1. Usable area is 17" x 23", gray area indicates 0.500" border for internal tooling area.
2. Green area indicates individual PCB.
3. Black area is 0.093" spacing for routing of individual PCBs. It is also acceptable to use 0.100" spacing.

Illustration B



1. Usable area is 16" x 22", gray area indicates 1.00" border for internal tooling area.
2. Green area indicates individual PCB.
3. Black area is 0.093" spacing for routing of individual PCBs. It is also acceptable to use 0.100" spacing.

*For PCBs or arrays that require scoring, PCBs are repeated center of shear line to center of shear line, as no spacing is required between PCBs.*

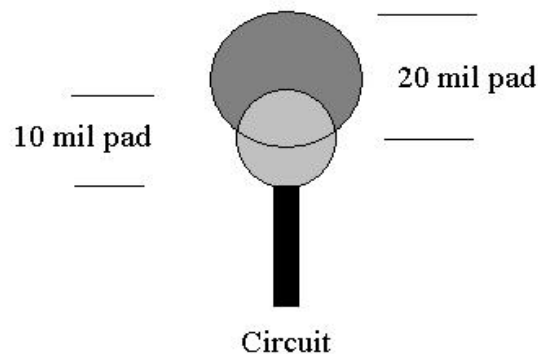
### **LINE WIDTHS AND SPACING**

Line widths and spacing are important considerations in achieving optimal yields. With today's technology demands, 5 mil line widths and 5 mil spacings can be achieved without additional cost adders. However, it is strongly recommended to allow for the greatest line width and size possible if the design can permit it. Our minimum line width and size would be 3 mils. In order to achieve 3 or 4 mils line width and spacing, it is usually necessary to process with a base Copper weight of 0.5oz.

### **DRILL**

This section will cover aspect ratio, annular ring, tear drop pads and inner layer clearances.

- Aspect Ratio – this is the PCB thickness divided by the hole diameter. If the PCB is 0.062” thick and requires 0.010” vias, then the aspect ratio would be 6.2:1. The highest aspect ratio we can build is 12:1. The optimal aspect ratio would be 6:1 or less.
- Annular Ring – this is the pad size in relationship to the hole size. Annular ring can be figured as pad size minus the hole size and then divided by two. If the pad size is 20 mils and the via size is 10 mils, then the annular ring would be 5 mils. Design features which permit greater than 5 mils annular ring are preferred and there is no maximum. The minimum annular ring would be 3 mils and it is strongly recommended to tear drop the pads (see tear drop pads).
- Tear Drop Pads – this is a method of producing a larger area for the critical junction of the circuit to the pad. This is accomplished by overlapping a smaller pad onto the via pad in the junction area. By implementing tear drop pads on tight annular ring requirements, it helps insure the best connection of circuit to via (as shown below):

**Tear Drop Pad**

- Inner Layer Clearance Pads – It is recommended to keep the clearance pads on internal layers 20 mils greater than the drill size. Since most manufacturer's drill 3~5 mils over the desired finish hole size (to allow for plating), then the clearance pad should be 20 mils + the drill size and not the finished hole size. For instance, to achieve a 20 mil hole, we will drill it with a 23 or 25 mil drill bit, therefore the internal clearance pads should be 43~45 mils or greater to achieve the optimal yields.

**MULTILAYERS**

When designing multilayers, the following should be considered:

- Always design in an even layer count, such as 4, 6, 8, 10...layers. This will produce a symmetrical lay up which in turn minimizes warp, not to mention that the price would be the same for a 5 layer PCB as a 6 layer PCB.
- The best layer to layer registration is +/- 0.003", however the typical tolerance is +/- 0.005".
- Stack ups should be left to the manufacturer to determine the most cost effective lay up. All multilayers should be symmetrical in stack up as shown below:

	<u>8 Layers</u>	<u>Target 0.062"</u>		<u>Mils</u>
Layer 1	Overplate (TL + Cu)	—————		1.5
	Copper Foil (0.5oz)	—————		0.7
Layer 2/3	Prepreg	1080		2.5
	Prepreg	1080		2.5
	Core	10 mil 1/1		12.8
	Prepreg	1080		2.5
Layer 4/5	Prepreg	1080		2.5
	Core	10 mil 1/1		12.8
	Prepreg	1080		2.5
	Prepreg	1080		2.5
Layer 6/7	Core	10 mil 1/1		12.8
	Prepreg	1080		2.5
	Prepreg	1080		2.5
	Prepreg	1080		2.5
Layer 8	Copper Foil (0.5oz)	—————		0.7
	Overplate (TL + Cu)	—————		1.5
			<b>Thickness</b>	<b>62.8</b>

An example of an unsymmetrical stack up would be as follows:

	<u>8 Layers</u>	<u>Target 0.062"</u>		<u>Mils</u>
Layer 1	Overplate (TL + Cu)	—————		1.5
	Copper Foil (0.5oz)	—————		0.7
Layer 2/3	Prepreg	1080		2.5
	Prepreg	1080		2.5
	Core	6 mil 1/1		8.8
	Prepreg	1080		2.5
Layer 4/5	Prepreg	1080		2.5
	Core	10 mil 1/1		12.8
	Prepreg	1080		2.5
	Prepreg	1080		2.5
Layer 6/7	Core	14 mil 1/1		16.8
	Prepreg	1080		2.5
	Prepreg	1080		2.5
	Prepreg	1080		2.5
Layer 8	Copper Foil (0.5oz)	—————		0.7
	Overplate (TL + Cu)	—————		1.5
			<b>Thickness</b>	<b>62.8</b>

A symmetrical stack up is achieved by balancing the top and bottom of the stack up equal in relationship to the center most core (in this example that would be Layer 4 and 5). Keep in mind that plane layers

should also follow this rule. Therefore if a power and ground plane are to be used, then if the power plane is on layer 2, the ground plane should be on layer 7.

### **SCREENING (SOLDERMASK & NOMENCLATURE)**

There are minimal concerns when considering soldermask and silk-screen design rules. Our standard process is LPI (liquid photoimageable) which produces the best registration around pad features. Typically soldermask should have a minimum of a 5 mil “growth” around the pad to allow for any mis-registration. And the minimum soldermask “dam” should be 6 mils (a dam is the minimum track size of soldermask). In respect to 20 mil pitch and smaller, we recommend a 1 mil “growth” to 0 mil, to allow for a sufficient “dam” size. Once the “dam” goes below 6 mils, it becomes more difficult to process without the “dam” lifting off the the PCB. Additionally, always cover via’s with soldermask that are directly beneath a surface mount device, like BGA’s or QFP’s. If the vias beneath the devices are not covered with soldermask, this could lead to unintentional solder bridging.

For silk-screen, the main consideration is font size. We recommend a 10 mil font minimum.

### **METALIZATION / SURFACE FINISH**

When selecting a surface finish, it is important to understand the assembly capabilities and process’s used. Below is a brief explanation of surface plating.

- Copper – all PCBs will be plated with Copper. The industry standard would be 1 mil of Copper plated over the base laminate Copper (with exception to inner layers which remain at the base Copper weight). When the PCB manufacturer selects drill sizes, they usually go 3~5 mils greater than the finished hole size to allow for plating.
- HASL – Hot Air Solder Level or Hot Air Level is the most cost effective method for surface finish over Copper. The typical thickness is 200~500 microinches. Although highly solderable and with minimal handling and storage requirements, it does not produce the best co-planor pad for SMT once the pitch gets to 25 mil or lesser. Although many assembly operations may not have trouble with HASL (Tin/Lead) an alternative surface finish such as

Immersion Silver, White Tin, ENIG or OSP may be more appropriate.

- Immersion Silver – just as it is stated, this process puts Silver over the Copper. The typical thickness is 3 to 8 microinches. Even though not as competitive as HASL, it does provide a more co-planar surface, but does require more considerations on handling and storage as it is more sensitive to environmental conditions. This process is great for 25 mil pitch and less.
- White Tin – almost identical to Immersion Silver. The real difference is assembly line preference.
- ENIG – Electroless Nickel Immersion Gold is a widely used surface finish for tight pitch SMT devices. It provides great solderability and co-planar pads, but tends to cost more than the White Tin and Immersion Silver process's.
- OSP – Organic Surface Protectant is a great surface finish as long as the assembly line can effectively set up to process. OSP is limited in its shelf life and handling is an issue. However, it does solder nicely and is environmentally friendly.

### **SUMMARY**

When designing and laying out PCBs it is important to consider features and processes that are both cost effective and adequate for their application. From a PCB manufacturer's view, bigger is still better, in terms of PCB features and the impact they have on our internal yields. If designs can permit 20 mil vias with 50 mil pads and 20 mil lines / spacing, then we encourage these designs. However, for those designs that are tight on space requirements, we hope the above will give some guidance as to the best way to lay out the PCB with the PCB manufacturer in mind.